REMARKS/ARGUMENTS

In the Office Action of July 27, 2006, the Examiner rejected claims 1 and 3-6 under 35 U.S.C. §102(b) as anticipated by Holmqvist (US 5,220,275). Further Examiner rejected claims 1, 3-6 and 9 under 35 U.S.C. §102(b) as anticipated by Summers (GB 2089601A). Claims 7-8 and 10-12 are rejected under 35 U.S.C. §103(a) as unpatentable over Ave (US 5359298) in view of Summers (GB 2089601A).

Examiner objected to claim 2 as dependent on a rejected claim but stated that the claim would be allowable if rewritten in independent form.

Applicants appreciate the time and consideration provided by the Examiner in reviewing this application and finding claim 2 to be allowable. Applicants respectfully traverse the rejections of claims 1 and 3-12 at least for the following reasons.

Rejection under 35 U.S.C. 102 (b)

The phase comparator circuit according to claim 1 of the present application includes four latch circuits L1 to L4. The phase comparator latches data signal Din at the rising edge of the clock signal CK1 in the latch L1, which designed to latch only the data whose sequential number coincides with even number. The data signal Din is latched at the rising edge of the clock signal CK2 in the latch L2, which designed to latch only the data whose sequential number coincides with odd number. The output of L1 is latched at the rising edge of the clock CK2 in the latch L3, and the output of L2 is latched at the rising edge of the clock CK1 in the latch L4 The output of latch L3 is used for delaying the data with sequential order coinciding with an even number in the data signal Din by T/2, and the output of latch L4 is used for delaying the data with sequential order coinciding with an odd number in the data signal Din by T/2, where the phase error is not present. An exclusive OR of the output from L2 and L3 is used as a first phase error signal, and exclusive OR of the output from L1 and L4 is used as a second phase error signal (See specification, page 10, line 8 through page 11, line 6, and Fig. 3).

In contrast, the phase digitizer according to Holmqvist includes four D-type flip-flops 31-34 clocked by a reference clock, where two D type flip-flops are positive edge

triggered, and the other two are negative edge triggered. (See column 7, lines 52-54, and Fig. 3). Similarly, the phase sensitive detector of Summers includes four D-type flip-flops 701 to 704 (Fig. 7, and page 3, lines 104-106). The operation of latches differs from the operation of the D type flip-flops. Enclosed Fig. 1 (corresponding to Fig. 4 of the present application) and Fig. 2 illustrate the difference in the operation of the phase comparator circuit according to the first embodiment of the present invention and the operation of the phase comparator circuits according to Holmqvist and Summers.

Based on the above, it is obvious that Claim 1 is novel and inventive in view of the cited prior art.

Moreover, Applicants respectfully submit that neither Holmqvist nor Summers disclose or suggest a phase comparator circuit for operating with a clock signal whose period is **2 times** the unit time width of an inputted data signal.

Figs. 3 and 5 present the time charts for illustrating the operation of the phase comparator circuit according to the present invention. The pulse width of Error 1 and Error 2 signals is varied by the phase error between the data signal Din and the clock signals CK1 and CK2 (See page 12, line 18-27 of the specification). As shown in Fig. 3, where the phase of CK1 (and CK2) gains by T/4 to the phase of Din, the pulse width of Error 1 (and Error 2) signal is shortened by T/4. As shown in enclosed Fig. 5, where the phase of CK1 (and CK2) delays for T/4 behind the phase of Din, the pulse width of Error 1 (and Error 2) signal is lengthened by T/4.

Figs. 4 and 6 enclosed herewith present the time charts for illustrating the operation of the phase comparator circuit according to Holmqvist and Summers. Fig. 4 illustrates that the phase of CK1 and CK2 gains by T/4 to the phase of Din, and Fig. 6 illustrates that the phase of CK1 and CK2 delays for T/4 behind the phase of Din. It could be seen that the two exclusive OR gates 35, 36 (in Holmqvist) and OR-gates 705, 706 (in Summers) do not output the pulse which has the pulse width varied by the phase error between the data signal and the clock signals CK1 and CK2.

Based on the above, Applicants respectfully submit that claims 3-6 and 9 are not anticipated by cited prior art.

Rejection under 35 U.S.C. 103(a)

Examiner rejected claims 7-8 and 10-12 as unpatentable over Abe (US 5,359,298) in view of Summers (GB 2089601A).

Abe discloses two CDR circuits. However, each of CDR circuits controls a separate VCC, that is, both CDR circuits operate in parallel. Abe neither discloses nor suggests two charge pump circuits wherein the source current flows into a loop filter according to the first and second phase error signals, and the sink current flows into the loop filter according to the first and second reference signals, and where they are designed to become equal with each other when the phase of the data signal Din and the phase of the clock signal CK1 and CK2 coincide with each other.

Applicants respectfully submit that claim 7, 8-and 10-12 are patentable and not obvious in view of the cited prior art references, or their combination.

The Examiner's indication of allowability for claim 2 is gratefully acknowledged.

Favorable consideration and allowance of claims 1 and 3 to 12, inclusive, in view of the preceding remarks appears in order and is respectfully urged.

The Commissioner is hereby authorized to charge any fees, which may be required in connection with this correspondence, to Deposit Account No. 06-1135.

Respectfully submitted,

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